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VERI Place Software Tool User Manual

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Software Version / Date	Release	Note
6.0 – 12.06.2014	VERI_Place	Xilinx Genesys board release (Virtex-5 V5LX50T)

1. Introduction

The VERI-Place tool is a software able to perform the Soft-Error Analysis and the Placement oriented to the Soft-Error mitigation of circuits on SRAM-based FPGAs. The software requires an OS based on the Ubuntu Linux (starting from the version 10.04).

The software includes the following features:

1. Overall logic resource exposure
2. Overall routing resource exposure
3. Global sensitivity bit report
4. Critical sensitivity heatmaps for programmable interconnection points (PIPs) and faulty conditions
5. Generation of the error rate report on the basis of bit-flip accumulation and expected Flip-Flops (FFs) minimal and maximal switching activity.

The version 6.0 is compatible with the Xilinx Virtex-5 XC5VLX50T. Further versions addressing different Xilinx families are available ***upon request from the user.***

The VERI-place tool requires a previous installation of the Xilinx ISE toolkit (starting from the version 13.6). In order to view some graphical file, you may require the installation of GIMP.

Important notices:

The VERI-Place tool available for download reports a bit reference ID number not referable to the Xilinx internal coordinate system.

It is not possible to use VERI-Place to directly decode Xilinx FPGA bitstream files.

2. VERI-Place Command line

The VERI-Place tool command line consists of:

VERI_PLACE [design XDL] [DRC UCF] [Option]

The [design XDL] is the XDL design file obtained through the generation of the XDL file by executing the command:

xdl –ncd2xdl design_name

The [DRC UFC] is the User Constraints File (UCF) file generated through the FPGA editor tool exporting the Direct Routing Constraints (DRC) information. The details on the generation of this command are described in the Section 3.

The [Option] corresponds to the kind of operation performed by the tool:

1 – analysis of the soft-error sensitivity of the circuits mapped on the FPGA. The analysis is executed performing a progressive accumulation of bit-flips (from 1 to 500) into the FPGA configuration memory. This analysis is executed at the lower switching activity of the design FFs.

The analysis 1 performs a preliminary sensitivity reports analyzing all the possible SEU effects within the FPGA configuration memory.

2 – analysis of the soft-error sensitivity of the circuit mapped on the FPGA. The analysis is executed performing a progressive accumulation of bit-flips (from 1 to 500) into the FPGA configuration memory. This analysis is executed at the higher switching activity of the design FFs.

3 – execution of the placement and re-packing operation.

3. Preparation of the input files

The generation of the input files requires the execution of some basic operations in order to create the files to be analyzed and elaborated by VERI-Place. In the present document the generation of the files and the related VERI-Place execution examples consider the elaborations applied to the B14 ITC benchmark implemented as plain design and using the X-TMR tool (Version 7.1). Both the versions are obtained with synthesis and implementation with the Xilinx ISE 14.1 suite on the Xilinx Virtex-5 XC5VLX50T. **Please consider that the tool can be used independently on a plain (not hardened) design as well as on a TMRed ones. The tool does not mandatorily need the plain and the XTMR versions.**

3.1 XDL file

The generation of the XDL file needs that the original design is preliminarily implemented on the selected FPGA device and the correspondent NCD file is available within the Xilinx ISE project folder.

Using the shell terminal, launch the following command:

xdl –ncd2xdl design.ncd (e.g., xdl –ncd2xdl b14.ncd)

After the execution of the XDL –NCD2XDL command, the design.xdl file will be available within the correspondent folder.

In Figure 1, it is illustrated the execution of the XDL command applied to the plain B14 design (B14) and to the XTMR ones (B14_XTMR).

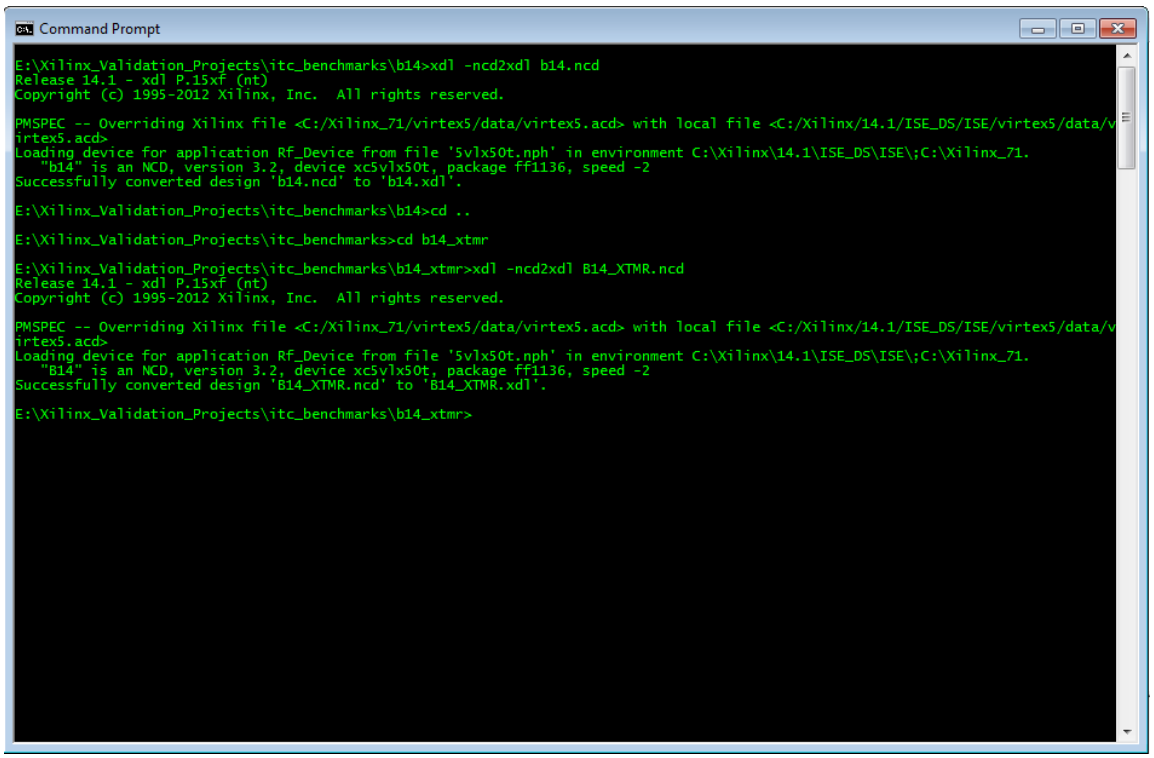

Figure 1. Execution of the XDL command for the B14 and B14-XTMR design examples.

3.2 DRC UCF file

The generation of the Directed Routing Constraints (DRC) UCF file requires the usage of the FPGA editor Xilinx tool. Once the NCD design is opened with FPGA editor, the steps for the generation of the UCF file are the following:

1. Tools – Directed Routing Constraints
2. Selects all the net in the DRC menu as illustrated in Figure 2
3. Please check that “Match routing exactly (ignore partially routed nets)”, “Append directed routing constraints to a file” and “Use Absolute Location Constraints” are checked
4. Define a proper UCF name (e.g., my_b14.ucf)
5. Click on “Apply”

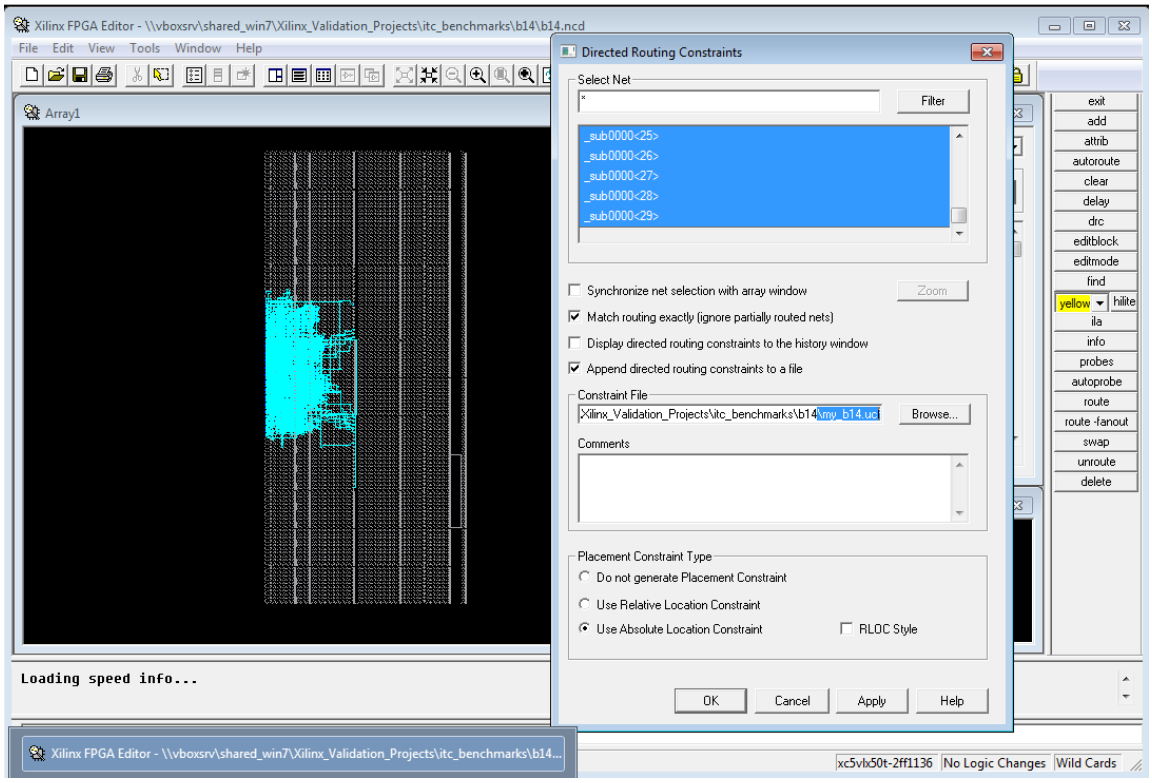

Figure 2. Example of generation of the DRC UCF file.

3.3 Preparation of the working directory

The preparation of the working directory requires a folder where the XDL file, the UCF file and the VERI-place executable are located. Therefore, create a directory and copy the three files within it.

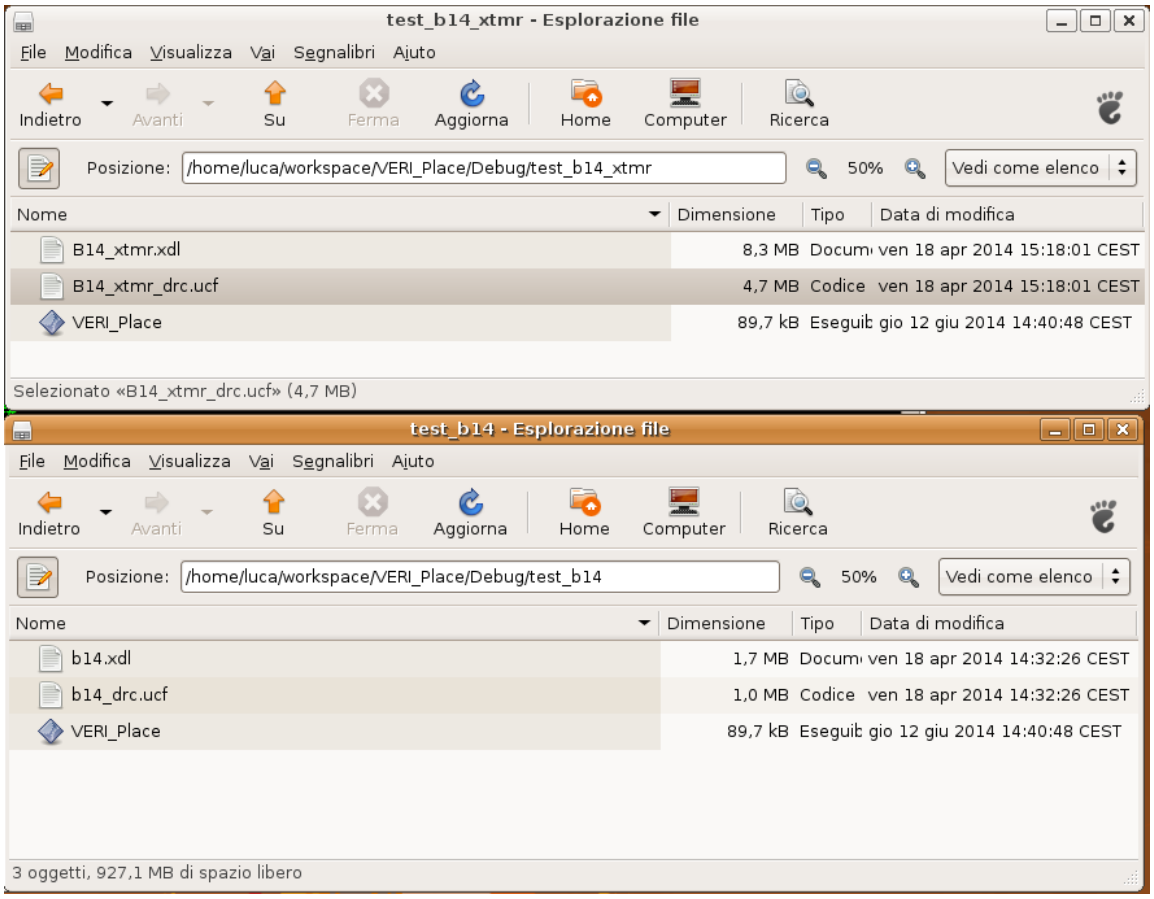

Figure 3. Example of the working directory status before the elaboration of VERI-Place.

4. Analysis of the Soft-Error Sensitivity

The analysis of the soft-error sensitivity can be executed by launching the VERI-Place tool with the following command line (option 1):

./VERI_place design.xdl design_drc.ucf 1

There are two options for the analysis of soft-errors: the option 1 is performing the analysis not considering the Flip-Flops switching activity, while option 2 is performing the analysis considering the maximal Flip-Flops switching activity.

As an example in Figure 4 it is reported the screenshot related to the loading of the B14 plain design.

Once VERI_place starts the execution it automatically executes the loading of the XDL file and of the UCF by reading and loading all the design information related to the logic resources and to the routing structure. Please note that the initial elaboration time may require some minutes.

At the end of the elaboration phase, the following information are displayed:

1. Potential Critical Condition Effects: A table listing different critical effects (see the annex pdf file of the user manual).
2. Heatmap layout level: A table with four different levels

3. The Static Analysis of the circuit resources: A report counting the sensitive bits related to the logic resources (logic) and to the routing resource (routing)

An example of such kind information, generated on the B14 plain design is illustrated in Figure 5 while to the B14-XTMR design in Figure 6.

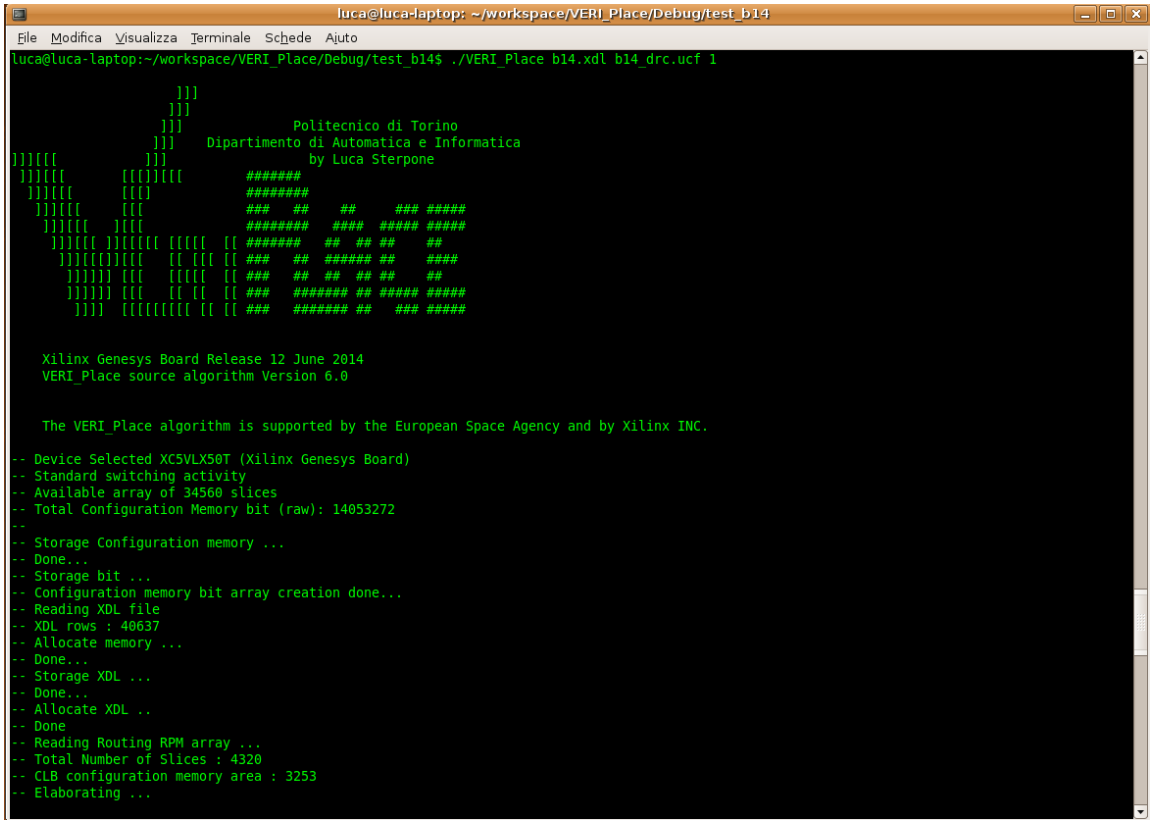

Figure 4. Example of the VERI-place screenshot during the design pre-elaboration.

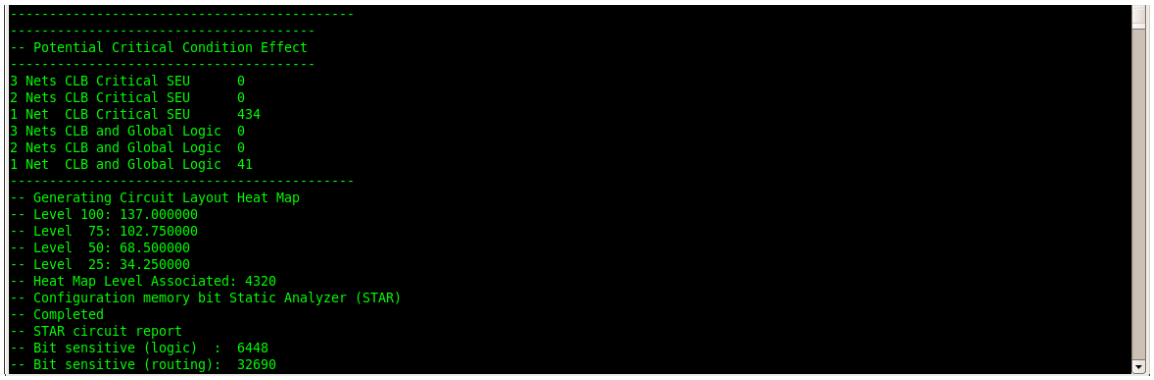

Figure 5. Example of the preliminary information data related to potential critical SEU effects related to the B14 plain design.

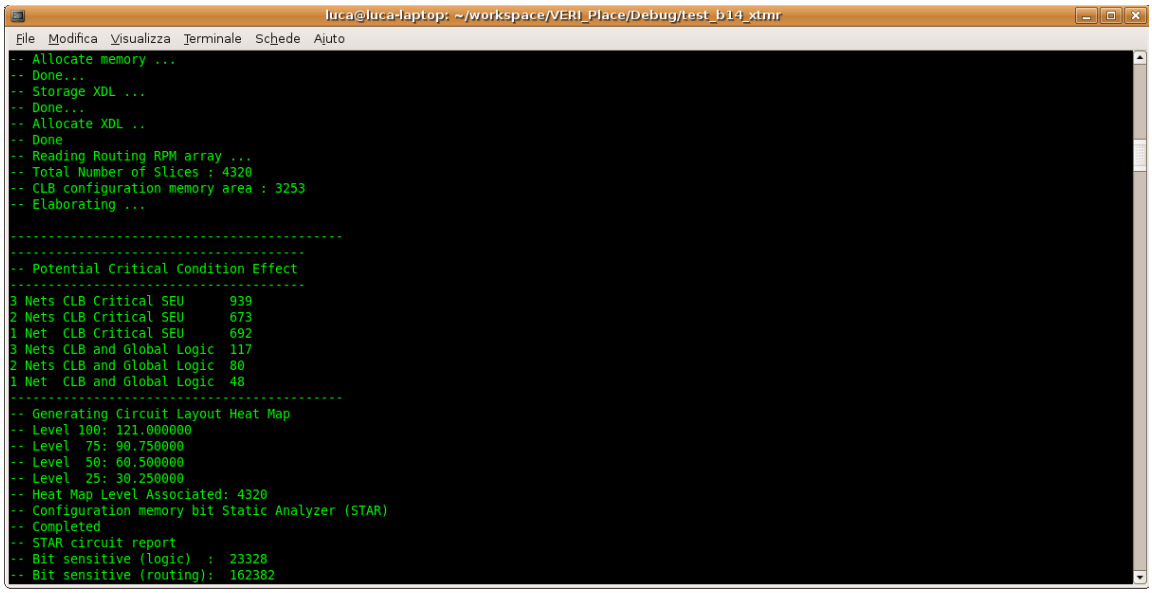

Figure 6. Example of the preliminary information data related to potential critical SEU effects related to the B14 XTMR design.

At the end of this phase, the VERI-place tool generates several report files:

1. DUT_ordered_exposure.txt: it contains the logic and routing resources related to each CLB. Each resource is considered as exposed to possible radiation effects, therefore the file reports the overall exposure of the implemented design ordered from the minimally exposed CLB to the maximally exposed CLB.
2. DUT_over_exposure.txt: it contains the logic and routing resources related to each CLB. It contains the same information of the DUT_ordered_exposure data file but it is ordered by CLB (from the X0Y0 CLB to the XNYM CLB, considering N and M the maximal number of CLB for the FPGA CLB rows and columns).
3. Heat_map_CONDITION.ppm: it represents a graphical visualization of the critical sensitivity area of the design (considering all FPGA resources). The colors criteria is the following:
    a. Black: not critical
    b. Blue: low criticality level
    c. Yellow: medium criticality level
    d. Red: high criticality level

    The “criticality level” can be considered as an index of the probability to have a failure inside of one of the identified locations.
4. DUT_cross_domain_exposure.txt (valid only for XTMR/TMR designs): it contains the logic and routing resources exposure that may provoke a Cross-Domain Failure affecting the X-TMR/TMR design structure. They are ordered from the minimally exposed CLB to the maximally exposed CLB.
5. Heat_map_PIP.ppm: it represents a graphical visualization of the interconnection congestion level of the considered design. Please consider that the color criteria is relative to the whole percentage of PIP and computed for each design:

a. Black: PIP count equal to 0.
b. Blue: 0 < PIP count <= 25%
c. Green: 25% < PIP count <= 50%
d. Yellow: 50% < PIP count <= 75%
e. Red: 75% < PIP count <= 100%

Please note that, if you need to compare two designs heat maps, you have to refer to the computed PIP level displayed by the VERI-Place tool during the generation layout heat map phase (as illustrated in Figure 5 and Figure 6).

Two examples of heat maps (conditions and PIP) related to the B14 plain and B14 XTMR are illustrated in Figure 7 and Figure 8.

6. STAR_sensitive_bits.txt (only option 1): it contains the list of sensitive bits reporting the bit reference, please note that the provided number is NOT referred to the FPGA bit-stream coordinate position, but it is consistent with the logic and routing FPGA coding.

   The file report the information in the following format:

   a. Routing resource:

      Bit reference number

      Routing resource name: PIP interconnection and PIP names (source and destination)

      Net name: name of the physical net-list

   b. Logic resource:

      Bit reference number

      Logic resource Name: kind of instance name, and CLB physical position

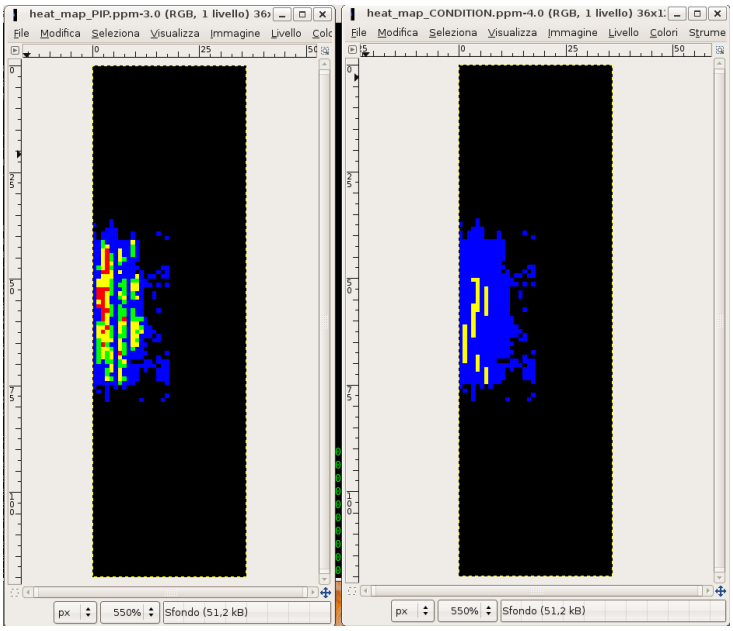

Figure 7. Example of PIP and CONDITION heat-maps generated by VERI-Place on the B14 plain design.

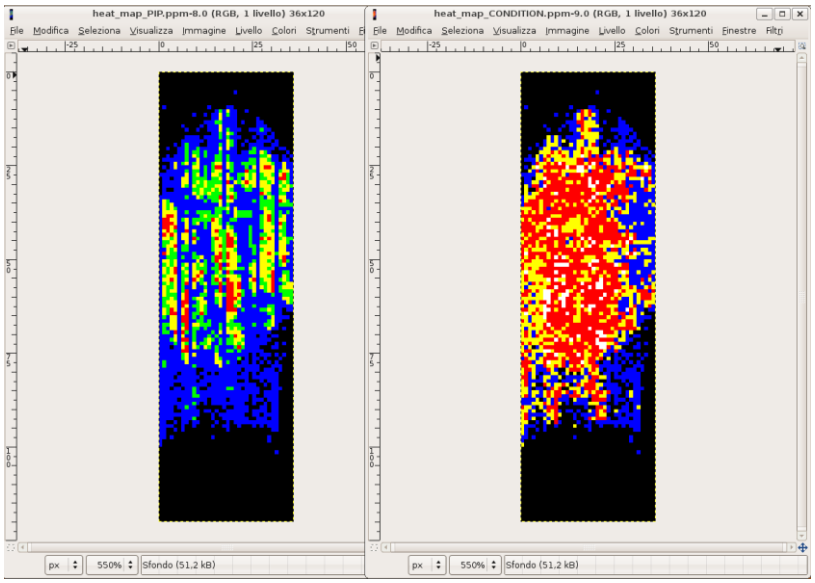

Figure 8. Example of PIP and CONDITION heat-maps generated by VERI-Place on the B14 XTMR design.

5. Note on the Sensitive Bits report

The results reported inside the STAR_sensitive_bits.txt include the number of logical and routing resources potentially critical to the implemented circuits. It does not correspond directly to the expected soft-error rate of the analyzed circuit. Considering the two circuits (B14 plain and B14 XTMR) the STAR_sensitive_bits reported are illustrated in the Figure 9, which plots the data contained in both the STAR_sensitive_bits files.

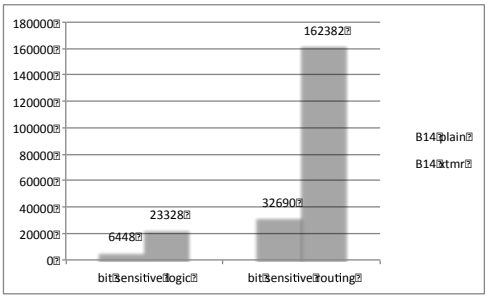

Figure 9. Example of PIP and CONDITION heat-maps generated by VERI-Place on the B14 XTMR design.

The data provided by the STAR sensitive bit file allows the identification of the effective configuration memory bits exposed to bit-flips that may critically affect the design behavior. For example, it is possible to observe the extreme high ratio between the exposed bits of the plain wrt the X-TMR version (XTMR sensitive bits / Plain sensitive bits = 6.55). *The STAR sensitive bit report does not provide* ***the expected Error Rate*** *of the implemented circuits, which requires the SEU progressive analysis performed by the VERI-Place tool described in the next section.*

6. VERI-Place SEUs progressive Error Rate analysis

The second phase, automatically executed by the VERI-Place tool, is the Error Rate computation, which is performed by a progressive Monte Carlo analysis. In details, VERI-Place analyzes the effects of SEUs within the configuration memory of Xilinx SRAM-based FPGA, by performing 60,000 random iterations (VERI-Place 6.0) of a number of SEUs ranging from 1 to 500 SEUs. For each number of SEUs it is calculated the expected error rate for both the plain circuit implementation and the X-TMR circuit implementation. The Error Rates are shown by the tool as “Plain-Error Rate” and “Cross-Domain Error Rate”. Please note that this computation may require some hours to be finalized.

The Error Rate is the ratio between the number of erroneous iterations and the total number of iterations. An erroneous iteration is identified once the analyzed configuration memory bits report an architectural modification that affects the circuit behavior provoking an error on the circuit outputs (independently from the circuit workload).

Please note that if VERI-Place is applied to a plain design (not TMR) the Cross-Domain Error Rate reported is fixed to 0.

The results of the progressive analysis is stored within the Error_Rate_Date.txt file.

An example of the analysis applied to the B14 plain design is reported in Figure 10, while in Figure 11 is observe the partial results when applied to the B14 XTMR.

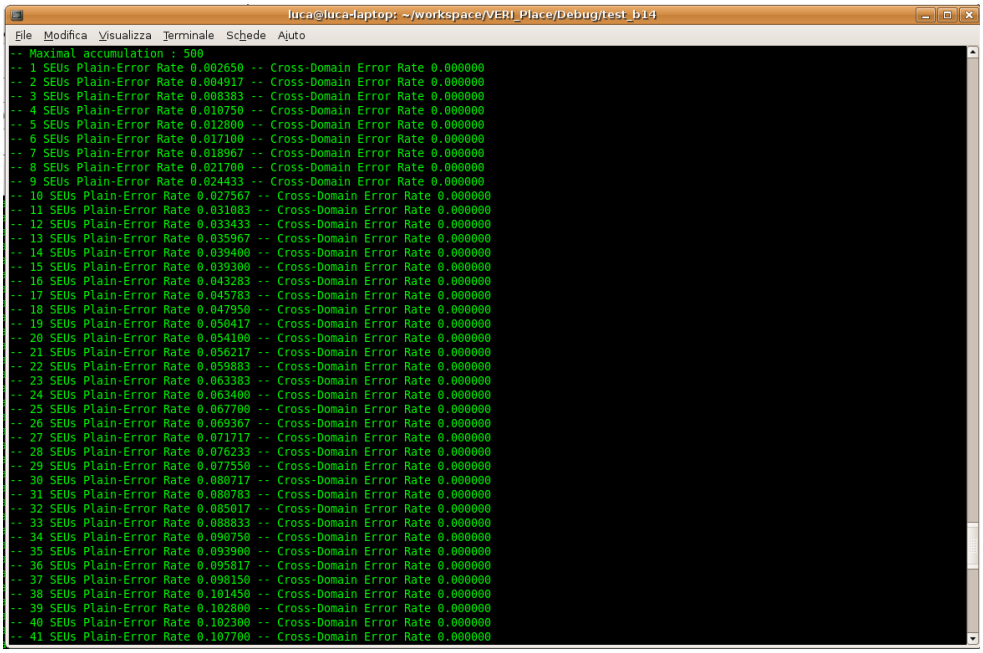

Figure 10. VERI-Place progressive Error Rate Computation Example on the B14 plain circuit.

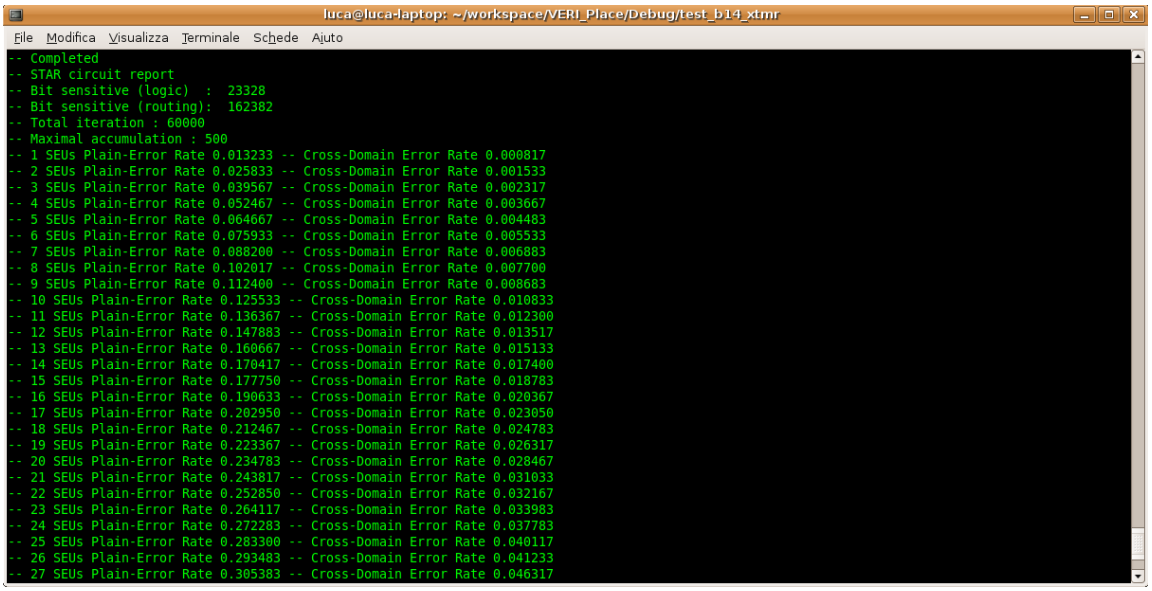

Figure 11. VERI-Place progressive Error Rate Computation Example on the B14 XTMR circuit.

6.1 The Error Rate Data file

The Error_Rate_Data.txt file contains the error rate results obtained using the progressive SEU analysis performed by the VERI-Place tool.

In details the file is generated on the basis of the following format:

#SEU;#Iterations;#Error Count Plain;#Error Count TMR

In order to plot the Error Rate, it is necessary to divide the “Error Count Plain” or the “Error Count TMR” columns with the number of iterations.

The Error Rate results generated applying the VERI-Place tool to the B14 Plain and B14 XTMR design is illustrated in Figure 12.

The Error Rate can be generated also using the option 2, which is considering the maximal switching activity for the user Flip-Flops.

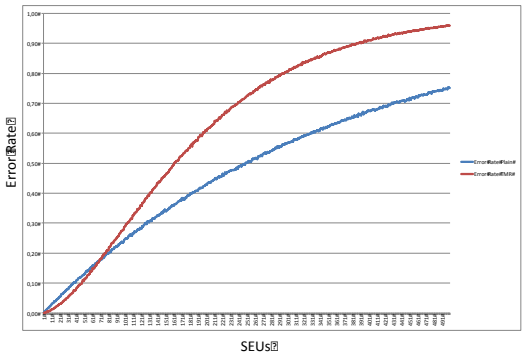

Figure 12. VERI-Place progressive Error Rate plots obtained on the B14 Plain and B14 TMR using Option 1 (low switching activity).

7. SEU Error Rate Circuit Investigation Methodology

In order to perform an effective analysis of a circuit SEU error rate, the following steps are suggested:

7.1. Analysis of the bit sensitivity

This analysis can be performed considering the data contained in the STAR_sensitivity_bits.txt. For our considered benchmark the comparison can provide information about the ratio of overhead bit resources used by the TMR hardened version with respect to the plain one. It is important to notice that the overhead bit introduced by any X-TMR or TMR solution is extremely different with respect to the resources overhead that can be estimated just by analyzing the circuit resources usage. As illustrated in Figure 13, it is possible to note that the X-TMR overhead for the B14 design is more than 6.5 times the B14 plain design.

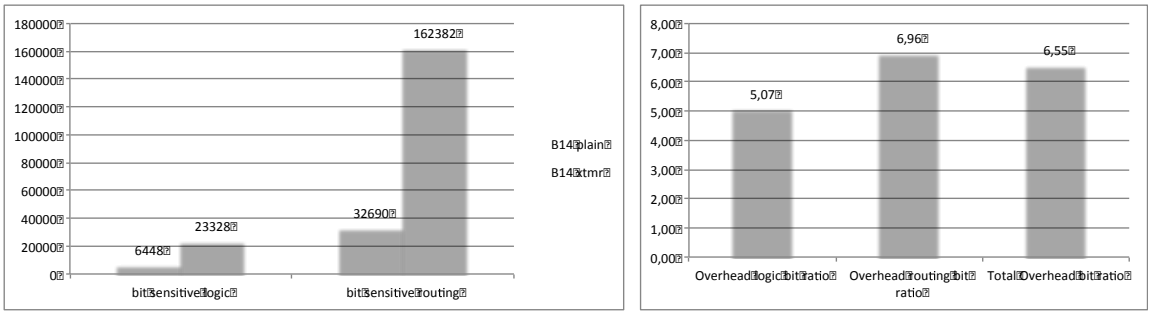

Figure 13. Information extracted using the STAR_sensitive_bits.txt report file on the B14 plain and B14 XTMR design.

7.2. Analysis and Verification of the Single Fault Assumption

This analysis is extremely important in order to individuate how many unique bit-flip may corrupt the implemented design. This data is provided within the Error Rate report considering the Error Rate when 1 SEU is analyzed. For the B14 examples, the results are illustrated in Figure 14.

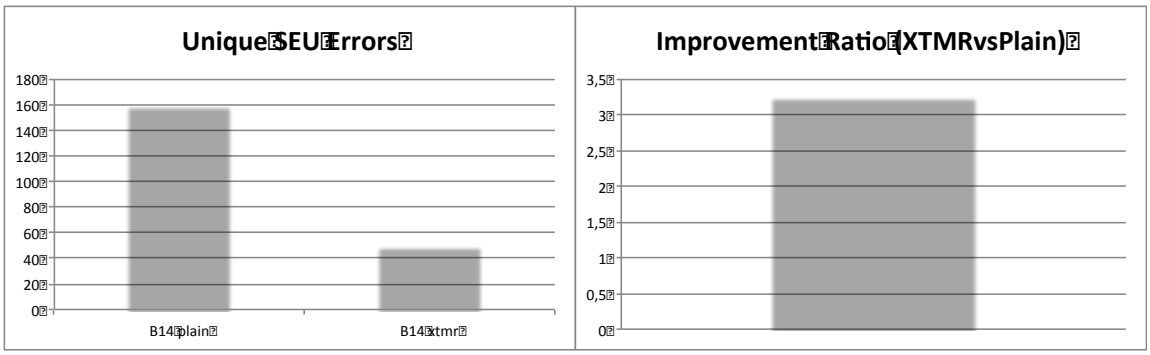

Figure 14. Single Event Upset sensitivity comparison and improvement ratio provided by the X-TMR tool.

7.3. Analysis of the SEU accumulation and identification of the breakeven point

This analysis is fundamental in order to identify the protection capability introduced by the mitigation methodology. In particular this can be analyzed considering the Error Rate plot and identifying the maximal different obtained using the mitigation methodology. As illustrated in Figure 15, it is possible to identify that the maximal error rate reduction is possible to be obtained once 28 Single Event Upsets are within the configuration memory. This data can be integrated

with the expected error rate (identifiable using the CREME96 software) and calculating the optimal reconfiguration or scrubbing time for the considered FPGA as well as the identification of the breakevent point, where the TMR mitigation solution results worst than the plain implementation.

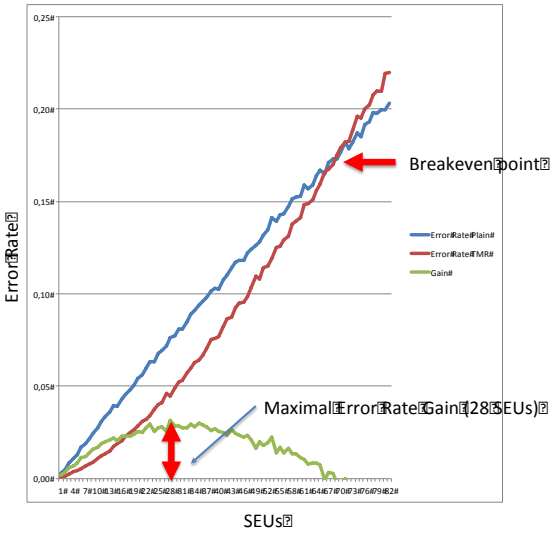

Figure 14. Error Rate plots on the B14 plain and B14 XTMR. Identification of the Maximal Error Rate Gain and of the SEU Breakeven Point.

7.4. Radiation-environment Error Rate Prediction

The VERI-Place tool can perform the Error Rate analysis in two different ways: considering a low circuit switching activity and a high (maximal) switching activity. This option can generate a double-plot error rate scenario, where effective radiation test data (dependent from a circuit workload) is predicted. As illustrated in Figure 15, an example of the data related to the B14 plain elaborated with the lower and higher switching activity.

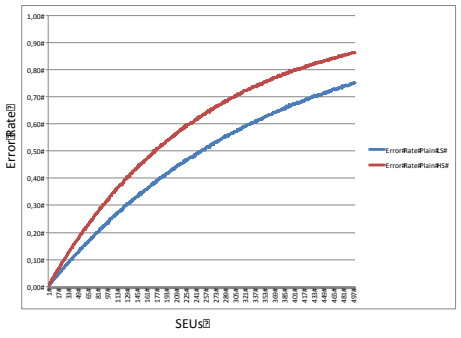

Figure 15. Error Rate Plots comparison between low and high switching activity. The “window” between the two lines allow to identify the effective error rate condition.

8. VERI-Place: repacking and replacement

The VERI-Place tool is able (option 3) to execute the replacement and repacking of the circuit in order to be compliant with the Single Fault Assumption full mitigation and to optimize the Maximal Error Gain with respect to the Plain and traditional X-TMR tool. It executes the following preliminary steps: placement status report and packing status report. Then it executes the following placement and re-packing phase:

1. Placement of CLB carry logic
2. Placement of CLB packed TMR
3. TMR packing
4. RAM resource checking
5. UCF packing generation
6. UCF area group generation

At the end of the placement phases two UCF files are generated:

1. **TMR_area_group.ucf**: this file contains the TMR area division performed on the basis of the TMR single fault assumption. This file can be included in the Xilinx ISE design flow in order to regenerate the FPGA design
2. **TMR_unpacking.ucf:** this file contains the low level packing of the CLB resource that can be placed on the FPGA using the PlanAhead Tool.